Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] 1.A reduced-input-capacitance bus switch comprising:
a bus-switch transistor, having a gate driven by an enable signal, a drain connected to a first input, and a source connected to a second input;
an isolated well under the bus-switch transistor, the isolated well isolated from a supply, the supply being a power source or a ground;
a well tap for electrically connecting to the isolated well;
a first well-shorting transistor, having a gate driven by the enable signal, a drain connected to the first input, and a source connected to the well tap;
a second well-shorting transistor, having a gate driven by the enable signal, a drain connected to the second input, and a source connected to the well tap; and
a biasing transistor, formed outside the isolated well, responsive to the enable signal or to an inverse of the enable signal, having a channel between the well tap and the supply that conducts current when the enable signal turns off the bus-switch transistor,
whereby the isolated well is shorted to the first and second input when the bus-switch transistor is turned on.

[c2] 2.The reduced-input-capacitance bus switch of claim 1 wherein a parasitic drain-to-well capacitor of the bus-switch transistor is shorted by the first well-shorting transistor when the enable signal turns on the bus-switch transistor;
wherein a parasitic source-to-well capacitor of the bus-switch transistor is shorted by the second well-shorting transistor when the enable signal turns on the bus-switch transistor,
whereby parasitic source-to-well and drain-to-well capacitors are shorted to reduce input capacitance.

[c3] 3.The reduced-input-capacitance bus switch of claim 2 wherein a doping concentration of the isolated well is at least two orders of magnitude less than a doping concentration of the source and the drain of the bus-switch transistor.

[c4] 4.The reduced-input-capacitance bus switch of claim 1 further comprising:
a metal line connecting the biasing transistor to the well tap.

[c5] 5.The reduced-input-capacitance bus switch of claim 4 wherein the well tap comprises a plurality of diffusion well tap regions having a same doping polarity as the isolated well, the well tap also comprising metal con-

ducting lines electrically connecting together two or more of the diffusion well tap regions.

[c6] 6.The reduced-input-capacitance bus switch of claim 5 wherein the biasing transistor has a drain connected to the well tap and a source connected to the supply.

[c7] 7.The reduced-input-capacitance bus switch of claim 6 wherein the bus-switch transistor, the first well-shorting transistor, and the second well-shorting transistor are n-channel transistors and wherein the isolated well is a P-well.

[c8] 8.The reduced-input-capacitance bus switch of claim 7 wherein the supply is the ground.

[c9] 9.The reduced-input-capacitance bus switch of claim 5 further comprising:
a second well of an opposite polarity type as the isolated well, the second well being formed under and surrounding the isolated well;
wherein a substrate is a same polarity type as the isolated well.

[c10] 10.The reduced-input-capacitance bus switch of claim 9 wherein the reduced-input-capacitance bus switch is formed using a triple-well process.

[c11] 11.The reduced-input-capacitance bus switch of claim 5 wherein the bus-switch transistor, the first well-shorting transistor, and the second well-shorting transistor are p-channel transistors and wherein the isolated well is an N-well, and wherein the supply is the power source.

[c12] 12.A bus switch comprising:
floating well means, in a substrate, for electrically isolating transistors formed within the floating well means from the substrate;
well tap means for electrically connecting to the floating well means;
a first input;
a second input;
an enable signal;
bus-switch transistor means, formed within the floating well means, for conducting current between the first input and the second input in response to the enable signal being in an enable state, and for isolating the first input from the second input in response to the enable signal being in an isolating state;
first well-shorting transistor means, formed within the floating well means, for conducting current between the first input and the well tap means in response to the enable signal being in the enable state to equalize voltages of the first input and the floating well means;

second well-shorting transistor means, formed within the floating well means, for conducting current between the second input and the well tap means in response to the enable signal being in the enable state to equalize voltages of the second input and the floating well means; and

well active-bias means, coupled to the well tap means, for biasing the floating well means to a supply voltage in response to the enable signal being in the isolating state.

[c13] 13.The bus switch of claim 12 wherein the well tap means comprises:

metal line means for conducting current;

diffusion tap means, having a same polarity type as the floating well means, for connecting to the metal line means.

[c14] 14.The bus switch of claim 13 wherein the well active-bias means comprises:

biasing transistor means, formed outside the floating well means, for conducting current between the supply voltage and the well tap means when the enable signal is in the isolating state.

[c15] 15.The bus switch of claim 14 further comprising:

first inverter means, receiving an enable input, for generating an inverse enable signal;

second inverter means, receiving the inverse enable signal, for generating the enable signal.

[c16] 16.The bus switch of claim 15 wherein the biasing transistor means has a gate that receives the inverse enable signal, while the bus-switch transistor means, the first well-shorting transistor means, and the second well-shorting transistor means each have a gate receiving the enable signal.

[c17] 17.The bus switch of claim 16 wherein the biasing transistor means is an n-channel transistor;
wherein the bus-switch transistor means is an n-channel transistor;
wherein the first and second well-shorting transistor means are n-channel transistors;
wherein the supply voltage is a ground; and
wherein the floating well means is a P-well.

[c18] 18.The bus switch of claim 16 wherein the biasing transistor means is a p-channel transistor;
wherein the bus-switch transistor means is a p-channel transistor;
wherein the first and second well-shorting transistor means are p-channel transistors;
wherein the supply voltage is a power supply; and
wherein the floating well means is an N-well.

[c19] 19.A bus switch device comprising:

a first input;

a second input;

an enable signal;

a power supply;

a ground;

an isolated P-well not directly connected to either the power supply or to the ground;

a first P+ well tap formed within the isolated P-well;

a second P-well directly connected to the ground by a second P+ well tap;

a bus-switch n-channel transistor having a gate driven by the enable signal, a first N+ source/drain connected to the first input, and a second N+ source/drain connected to the second input, the bus-switch n-channel transistor formed within the isolated P-well;

a first well-shorting n-channel transistor having a gate driven by the enable signal or a logical equivalent to the enable signal, a first N+ source/drain connected to the first input, and a second N+ source/drain electrically connected to the isolated P-well through the first P+ well tap, the first well-shorting n-channel transistor formed within the isolated P-well;

a second well-shorting n-channel transistor having a gate driven by the enable signal or a logical equivalent to

the enable signal, a second N+ source/drain connected to the second input, and a second N+ source/drain electrically connected to the isolated P-well, the second well-shorting n-channel transistor formed within the isolated P-well; and

a biasing n-channel transistor, formed outside the isolated P-well, for connecting the isolated P-well to the ground when the enable signal disables the bus-switch n-channel transistor.

[c20] 20.The bus switch device of claim 19 wherein a plurality of bus switch devices are integrated together onto a single silicon chip.